CA-IS3082WW 7.5kV$_{RMS}$ Reinforced Isolated Half-Duplex RS-485 Transceiver in an Ultra-Wide-Body SOIC Package

1 Key Features

- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- 500kbps Data Rate
- 1/8 Unit Load (Up to 256 Bus Nodes)
- Logic-Side Supply Voltage: 2.375V to 5.5V
- Bus-Side Supply Voltage: 3V to 5.5V
- Common Mode Range on Bus Pins: –7V to +12V
- High CMTI: ±150kV/μs (typ)
- Bus Pins (A/B) ESD Protection: ±20kV (HBM)
- Driver with Current Limiter and Thermal Shutdown Protection
- Open, Short and Idle Bus Failsafe Protection
- Extended Industrial Temperature Range: –40°C to 125°C
- 16-Pin Ultra-Wide-Body SOIC Package, creepage and clearance ≥ 15mm
- > 40-Year Lifetime at Rated Isolated Voltage
- Safety-Related Certifications (Pending):
  - VDE certification per DIN EN IEC 60747-17 (VDE 0884-17):2021-10
  - UI certification per UL 1577
  - CQC certification per GB4943.1-2022 standards
  - TUV certification

2 Applications

- Solar Inverter
- High Voltage Energy Storage Systems
- Railway Transportation
- Wind Power System
- Charging Pile

3 Description

The CA-IS3082WW devices are reinforced isolated RS-485 transceivers which have excellent performance to meet the needs of the industrial applications. All devices of this family have the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides up to 7.5-kV_{RMS} (60s) of galvanic isolation of and typical ±150kV/μs CMTI. Isolation barrier improves communication quality by breaking ground loops and reducing noise where there are large differences in ground potential between ports.

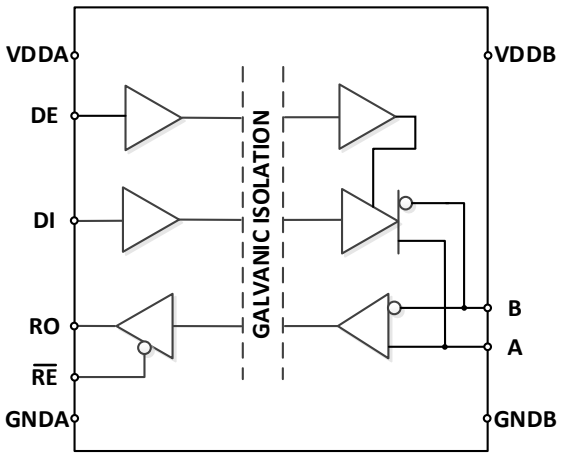
The CA-IS3082WW devices support multi-node data communication, and maximum data rate is up to 500kbps, allowing up to 256 transceivers (loads) on a common bus. The CA-IS3082WW devices are half-duplex transceivers, which could control the driver and receiver enable pins to avoid bus conflicts.

The CA-IS3082WW devices are available in 16-pin ultra-wide-body SOIC package (creepage and clearance ≥ 15mm), and specified over extended industrial temperature range of –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS3082WW	SOIC16-WWB (WW)	10.3mm × 14.00mm

Simplified Block Diagram



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	VDDA (V)	VDDB (V)	Full/half-duplex	Date Rate (kbps)	Isolation Rating (V_{RMS})	Package
CA-IS3082WW	2.375~5.5	3.0~5.5	Half-duplex	500	7500	SOIC16-WWB

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5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2024/09/24	NA

6 Pin Descriptions and Functions

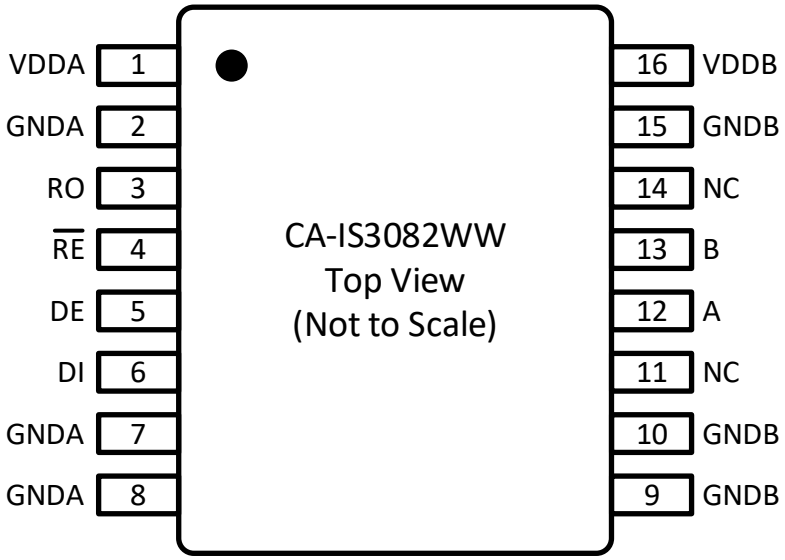


Figure 6-1 Pin Configuration

Table 6-1 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
VDDA	1	Power supply	Logic-side power input. Bypass VDDA to GNDA with both 0.1µF and 1µF capacitors as close to the device as possible.
GNDA	2, 7, 8	Ground	Logic-side ground. GNDA is the ground reference for digital signals.
RO	3	Digital Output	Receiver data output. Drive $\overline{RE}$ low to enable receiver. With $\overline{RE}$ low, RO is high when ($V_A - V_B$) ≥ –50mV and is low when ($V_A - V_B$) ≤ –200mV.
$\overline{RE}$	4	Digital Input	Receiver output enable, pulled up internally. Driver $\overline{RE}$ low or connect it to GNDA to enable receiver. Drive $\overline{RE}$ high to disable receiver.
DE	5	Digital Input	Driver output enable, pulled down internally. Drive DE high to enable driver. Drive DE low or connect it to GNDA to disable driver.
DI	6	Digital Input	Driver input, pulled up internally. With DE high, a logical low on DI forces the non-inverting output (A) low and the inverting output (B) high; a logical high on DI forces the non-inverting output high and the inverting output low.
GNDB	9, 10, 15	Ground	Bus side ground. GNDB is the ground reference for the RS-485 bus signals.
NC	11, 14	--	No internal connection, could connect it to VDDB or GNDB or leave it open.
A	12	Bus I/O	Non-inverting receiver input and driver output.
B	13	Bus I/O	Inverting receiver input and driver output.
VDDB	16	Power supply	Bus side power input. Bypass VDDB to GNDB with both 0.1µF and 1µF capacitor as close to the device as possible.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage[2]	–0.5	6.0	V
V_{IO}	Bus voltage of A and B[2]	–8	13	V
V_{IO}	Logical voltage of DI, DE $\overline{RE}$ and RO	–0.5	V_{DDA} + 0.5[3]	V
I_{IO}	Output current of RO	–20	20	mA
T_J	Junction Temperature	–40	150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values except differential I/O bus voltages are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 6V.

7.2 ESD Ratings

PARAMETER			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins (A, B) to GNDB	±20	kV
		Bus-side other pins to GNDB	±6	
		All logic-side pins to GNDA	±6	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{DDA}	Logic-side supply voltage, with respect to GNDA	2.375	3.3 or 5.0	5.5	V
V_{DDB}	Bus-side supply voltage, with respect to GNDB	3.0	3.3 or 5.0	5.5	V
V_{OC}	Common mode voltage on bus pins (A, B)	–7		12	V
V_{ID}	Differential input voltage between A and B	–12		12	V
R_L	Differential load resistance	54			Ω
V_{IH}	High-level input voltage of DI, DE	2.0		V_{DDA} + 0.3	V
V_{IL}	Low-level input voltage of DI, DE	–0.3		0.8	V
V_{IH}	High-level input voltage of $\overline{RE}$	0.7 × V_{DDA}		V_{DDA} + 0.3	V
V_{IL}	Low-level input voltage of $\overline{RE}$	–0.3		0.3 × V_{DDA}	V
I_{IO}	Output current of RO	–8		8	mA
DR	Data Rate			500	kbps
T_A	Ambient Temperature	–40		125	°C
T_J	Junction Temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC		PACKAGE	UNIT
		SOIC16-WWB (WW)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.3	°C/W

7.5 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	> 15	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	> 15	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $300V_{RMS}$	I-IV	
		Rated mains voltage ≤ $600V_{RMS}$	I-IV	
		Rated mains voltage ≤ $1000V_{RMS}$	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2828	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	2000	V_{RMS}
		DC voltage	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	10600	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	9846	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin(2πft), f = 1MHz	~ 0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	7500	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.6 Safety-Related Certifications

VDE(Pending)	UL (Pending)	CQC(Pending)	TUV(Pending)
Certified according to DIN EN IEC 60747-17(VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Reinforced insulation V_{IORM}: 2828V_{PK} V_{IOTM}: 10600V_{PK} V_{IOSM}: 12800V_{PK}	Single protection 7500V_{RMS}	reinforced isolation (Altitude ≤ 5000m)	EN 61010-1: 7500V_{RMS} EN 62368-1: 7500V_{RMS}
Certification Number: Pending	Certification Number: Pending	Certification Number: Pending	Certification Number: EN 61010-1: Pending EN 62368-1: Pending

7.7 Electrical Characteristics

7.7.1 Driver

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{DDA} = V_{DDB} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD1}\|$	Differential output voltage	V_{DDB} = 5V, no load	2.7	4.6	5.5	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 54Ω, C_L = 50pF, see Figure 8-1	1.5	3.6		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential-output voltage		–0.2		0.2	
V_{OC}	Common-mode output voltage		1	V_{DDB}/2	3	
ΔV_{OC}	Change in magnitude of common-mode output voltage		–0.2		0.2	
I_{IH}, I_{IL}	Input current (DI, DE)	DI or DE = 0V or V_{DDA}	–20		20	µA
I_{OS}	Driver short-circuit output current	DE = V_{DDA}, V_A or V_B = –7V	–150		150	mA
		DE = V_{DDA}, V_A or V_B = 12V				
CMTI	Common mode transient immunity	V_{CM} =1000V, see Figure 8-8	±100	±150		kV/µs

7.7.2 Receiver

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{DDA} = V_{DDB} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Positive-going input threshold voltage threshold			–110	–50	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage threshold		–200	–140		mV
$V_{IT(HYS)}$	Receiver input hysteresis			30		mV
I_I	Bus input current	V_A or V_B = 12V, V_{DDB} = 3.3V or 5V, other logic input pins are connected to 0V		75	125	µA
		V_A or V_B = 12V, V_{DDB} = 0V, other logic input pins are connected to 0V		80	125	
		V_A or V_B = –7V, V_{DDB} = 3.3V or 5V, other logic input pins are connected to 0V	–100	–40		
		V_A or V_B = –7V, V_{DDB} = 0V, other logic input pins are connected to 0V	–100	–40		
R_{ID}	Bus input resistance	Between A and B	96			kΩ
I_{IH}, I_{IL}	Input current ($\overline{RE}$)	$\overline{RE}$ = 0V or V_{DDA}	–20		20	µA
V_{OH}	Output voltage high level	V_{DDA} = 5V, I_{OH} = –4mA	V_{DDA} – 0.4	V_{DDA} – 0.2		V
V_{OL}	Output voltage low level	V_{DDA} = 5V, I_{OL} = 4mA		0.2	0.4	V
C_{ID}	Bus differential input capacitance	V_I = 0.4V × sin(2πft), f = 1MHz, between A and B		12		pF
C_{IN}	Bus single-ended input capacitance	V_I = 0.4V × sin(2πft), f = 1MHz, A or B to GNDB		18		pF
CMTI	Common mode transient immunity	V_{CM} =1000V, see Figure 8-8	±100	±150		kV/µs

7.7.3 Supply Current

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{DDA} = V_{DDB} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DDA}	Logic-side supply current	$\overline{RE}$ = 0V or V_{DDA}, DE = V_{DDA}	DI = V_{DDA}	V_{DDA} = 3.3V		2.9	4.6	mA
				V_{DDA} = 5V		3.0	4.6	
		$\overline{RE}$ = 0V or V_{DDA}, DE = 0V		V_{DDA} = 3.3V		1.6	3.0	
				V_{DDA} = 5V		1.7	3.0	
		$\overline{RE}$ = 0V or V_{DDA}, DE = V_{DDA}	DI = 0V	V_{DDA} = 3.3V		4.2	7.0	
				V_{DDA} = 5V		4.3	7.0	
		$\overline{RE}$ = 0V or V_{DDA}, DE = 0V		V_{DDA} = 3.3V		2.8	4.4	
				V_{DDA} = 5V		2.9	4.4	
I_{DDB}	Bus-side supply current	$\overline{RE}$ = 0V or V_{DDA}, DE = V_{DDA}	DI = V_{DDA}, no load between A and B	V_{DDA} = 3.3V		3.0	4.6	
				V_{DDA} = 5V		3.1	4.6	
		$\overline{RE}$ = 0V or V_{DDA}, DE = 0V		V_{DDA} = 3.3V		2.7	4.2	
				V_{DDA} = 5V		2.8	4.2	
		$\overline{RE}$ = 0V or V_{DDA}, DE = V_{DDA}	DI = 0V, no load between A and B	V_{DDA} = 3.3V		4.2	7.0	
				V_{DDA} = 5V		4.3	7.0	
		$\overline{RE}$ = 0V or V_{DDA}, DE = 0V		V_{DDA} = 3.3V		2.6	4.2	
				V_{DDA} = 5V		2.7	4.2	

7.8 Timing Characteristics

7.8.1 Driver

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{DDA} = V_{DDB} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Driver Propagation Delay	See Figure 8-2 and Figure 8-3		100	250	ns
t_{PWD}	Driver output skew $\lvert t_{PLH} - t_{PHL} \rvert$			5	20	ns
t_r	Differential output rise time			135	500	ns
t_f	Differential output fall time			135	500	ns
t_{PZH}, t_{PZL}	Driver enable time	See Figure 8-7		24	180	ns
t_{PHZ}, t_{PLZ}	Driver disable time			24	60	ns

7.8.2 Receiver

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{DDA} = V_{DDB} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Receiver Propagation Delay	See Figure 8-4 and Figure 8-5		80	160	ns
t_{PWD}	Receiver output skew $\lvert t_{PLH} - t_{PHL} \rvert$				20	ns
t_r	Receiver output rise time			2.5	4	ns
t_f	Receiver output fall time			2.5	4	ns
t_{PHZ}, t_{PLZ}	Receiver enable time	See Figure 8-6		12	25	ns
t_{PZH}, t_{PZL}	Receiver disable time, DE = 0V			12	25	ns

8 Parameter Measurement Information

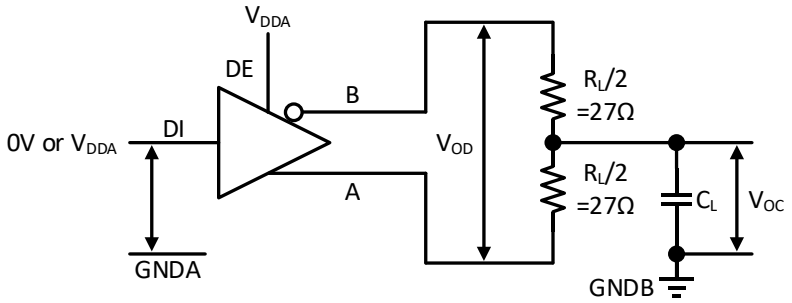
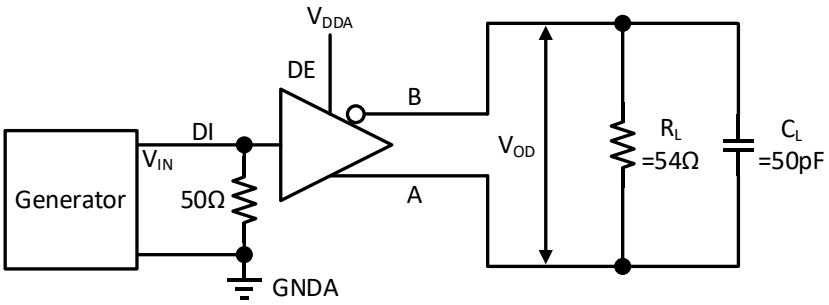


Figure 8-1 Driver DC Test Circuit



Note:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125kHz, 50% duty cycle; rise time t_r ≤ 6ns, fall time t_f ≤ 6ns; Z_O = 50Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance

Figure 8-2 Driver Propagation Delay Test Circuit

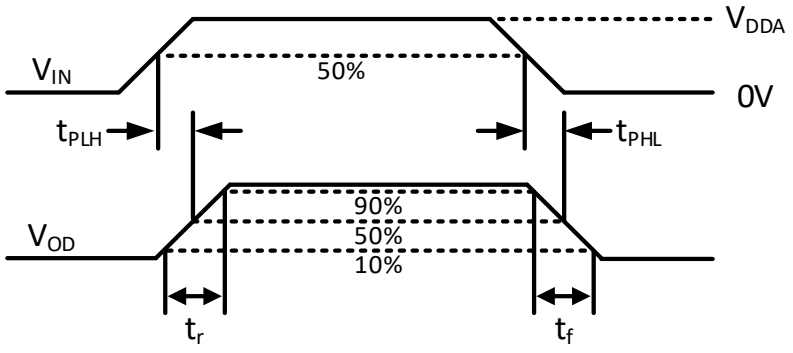
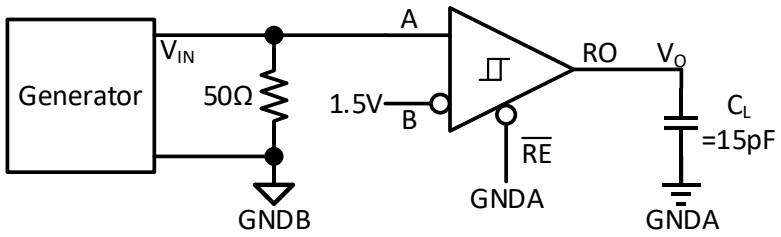


Figure 8-3 Driver Output Rise and Fall Time and Propagation Delay



Note:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125kHz, 50% duty cycle; rise time t_r ≤ 6ns, fall time t_f ≤ 6ns; Z_O = 50Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance

Figure 8-4 Receiver Propagation Delay Test Circuit

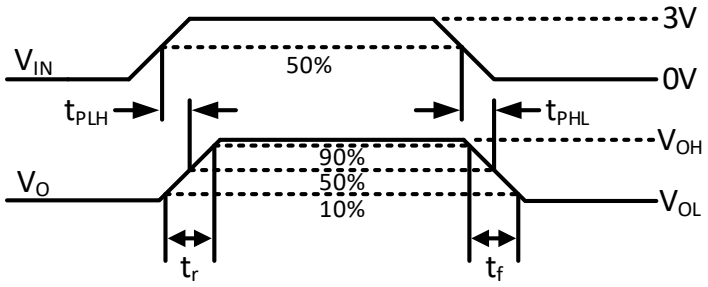


Figure 8-5 Receiver Output Rise and Fall Time and Propagation Delay

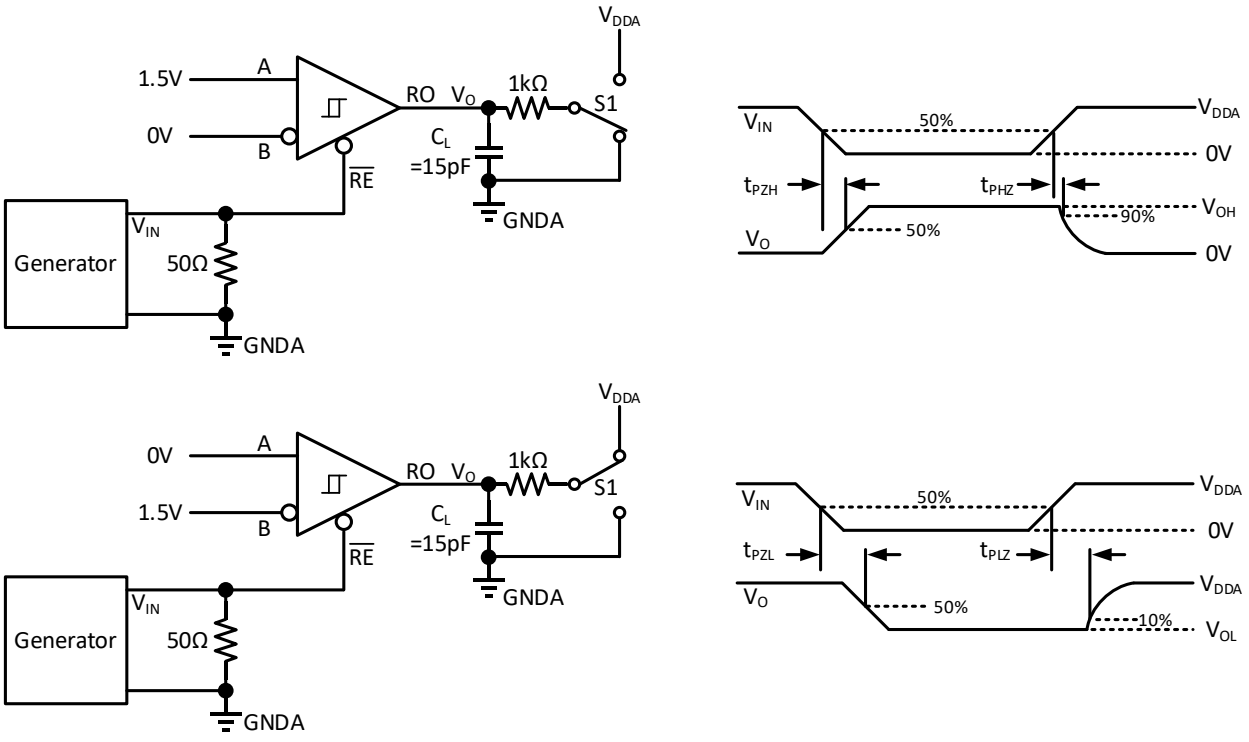


Figure 8-6 Receiver Enable and Disable Time

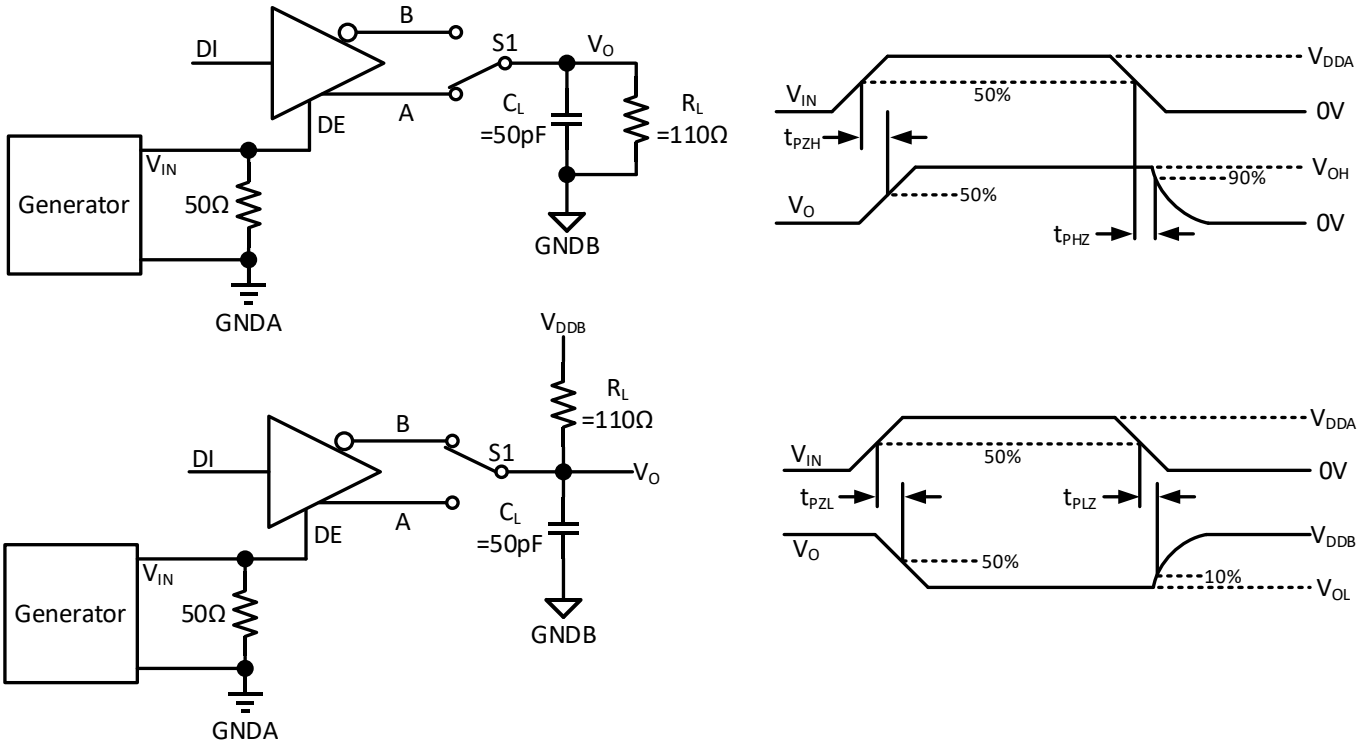


Figure 8-7 Driver Enable and Disable Time

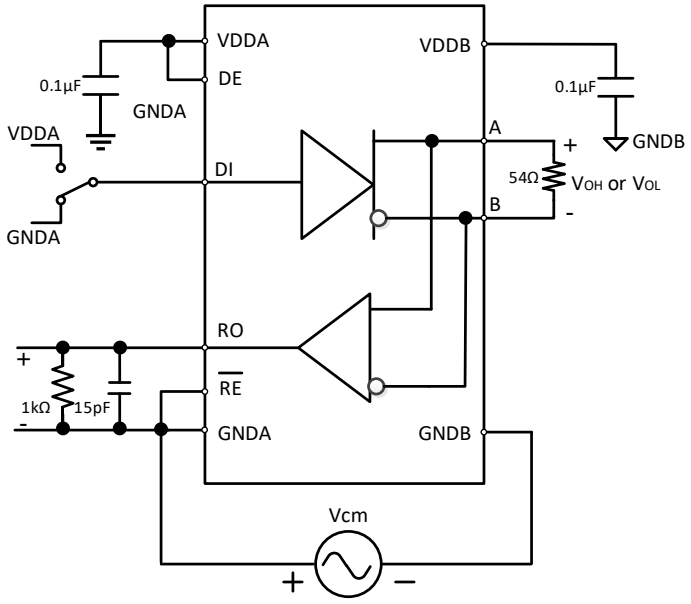


Figure 8-8 Common Mode Transient Immunity (CMTI) Test Circuit

9 Detailed Description

9.1 Overview

The CA-IS3082WW reinforced isolated RS-485 transceivers provide up to 7.5-kV_{RMS} of galvanic isolation between the cable side (bus side) of the transceiver and the controller side (logic side). These devices feature ±150-kV/μs (typ) common mode transient immunity, allowing up to 500-kbps date rate across the isolation barrier. Robust isolation performance with extended ESD protection enables reliable communication in noisy environments, making these devices ideal for a wide range of industrial applications, such as motor drives, High Voltage Energy Storage Systems, railway Transportation, wind Power System, and Charging Pile. There exist two mechanisms against excessive power dissipation caused by faults or bus contention. The first, a current limiter on the output stage of the driver, providing immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit forces the driver outputs into a high-impedance state once the junction temperature exceeds $T_{J(shutdown)}$.

9.2 Logic Input

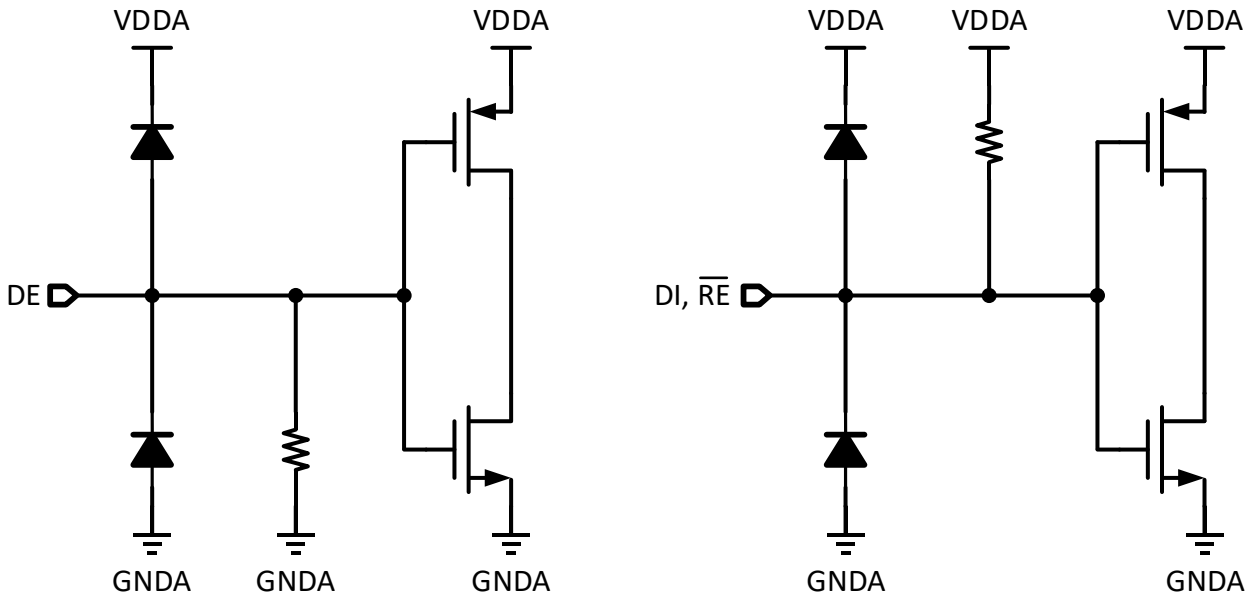


Figure 9-1 Logic Input Equivalent Circuit

The CA-IS3082WW isolated RS-485 transceivers include three logic inputs on the logic side: receiver enable pin $\overline{RE}$, driver enable pin DE and driver digital input pin DI. The driver enable pin DE is weakly pulled down to GNDA internally, while the digital input DI pin and receiver enable $\overline{RE}$ pin are weakly pulled up to VDDA internally. The logic input equivalent circuit is shown in Figure 9-1.

9.3 Receiver

The receiver detects the differential input from the bus line (A and B) and transfers it to a single-ended output RO to the logic-side controller. When the receiver enable pin $\overline{RE}$ is set to low, receiver is enabled. When the receiver enable pin $\overline{RE}$ is set to high, receiver is disabled. The truth table of CA-IS3082WW's receiver is shown in Table 9-1.

In case the receiver has been enabled, if the differential input voltage $V_{ID} = V_A - V_B$ is higher than or equal to the threshold voltage $V_{IT+(IN)}$, receiver output RO is logical high. Conversely, if the differential input voltage V_{ID} is lower than or equal to the threshold voltage $V_{IT-(IN)}$, receiver output RO is logical low. If the differential input voltage V_{ID} is between $V_{IT+(IN)}$ and $V_{IT-(IN)}$, receiver output RO is indeterminate.

When $\overline{RE}$ is logical high or open, the receiver is disabled and the output RO is high-impedance and is irrelevant to the magnitude and polarity of V_{ID}.

When the bus inputs are open, short or on idle state, a failsafe logic high output at RO pin is achieved, and the external fail-safe bias resistors could be eliminated.

Table 9-1 Truth Table of Receiver[1]

VDDA	VDDB	DIFFERENTIAL INPUT	ENABLE	OUTPUT
		$V_A - V_B$	$\overline{RE}$[2]	RO
PU	PU	$V_{IT+(IN)} \le V_A - V_B$	L	H
		$V_{IT-(IN)} < V_A - V_B < V_{IT+(IN)}$	L	Indeterminate
		$V_A - V_B \le V_{IT-(IN)}$	L	L
		X	H	Hi-Z
		X	Open	Hi-Z
		Open/Short/Idle	L	H
PD	PU	X	X	Hi-Z
PU	PD	X	L	H

NOTE:
1. H = high level, L = low level, X = irrelevant, High-Z = high impedance, PD = powered down, PU = powered up.
2. $\overline{RE}$ is weakly pulled up to VDDA internally.

9.4 Driver

The driver converts the single-ended input signal (DI) from the local controller to the differential outputs for the bus lines A and B. The truth table of driver is shown in Table 9-2. The driver outputs and receiver inputs are protected by ±20-kV electrostatic discharge (ESD) to GNDB on the bus side, as specified by the Human Body Model (HBM). The driver outputs also feature current limiting and thermal shutdown protection. The DE pin of driver is weakly pulled down to GNDA internally, thus the driver is disabled when the DE pin is floating. The DI pin of driver is weakly pulled up. When the driver is enabled, the driver outputs high level if DI is floating.

Table 9-2 Truth Table of Driver[1]

VDDA	VDDB	LOGIC INPUT	ENABLE INPUT	OUTPUTS	
		DI[2]	DE[3]	A	B
PU	PD	H	H	H	L
		L	H	L	H
		X	L	Hi-Z	Hi-Z
		X	Open	Hi-Z	Hi-Z
		Open	H	H	L
PD	PU	X	X	Hi-Z	Hi-Z
PU	PD	X	X	Hi-Z	Hi-Z
PD	PD	X	X	Hi-Z	Hi-Z

NOTE:
1. H = high level, L = low level, X = irrelevant, High-Z = high impedance, PD = powered down, PU = powered up.
2. DI is weakly pulled up to VDDA internally.
3. DE is weakly pulled down to GNDA internally.

9.5 Device Protection Functions

9.5.1 Signal Isolation

The CA-IS3082WW devices integrate digital galvanic isolators using capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allowing data transmission between the logical side and bus side of the transceiver with 7.5-kV_{RMS} isolation rating.

9.5.2 Thermal Shutdown Protection

If the junction temperature of the CA-IS3082WW device exceeds the thermal shutdown threshold $T_{J(shutdown)}$ (175°C, typ), the driver is disabled and the driver outputs go high-impedance state. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.5.3 Current Limiting Protection

The CA-IS3082WW devices protect the driver output stage against a short circuit to a positive or negative voltage over the common mode voltage range from –7V to 12V by limiting the driver output current. However, this could cause large supply current and dissipation, as well as result in the rising of junction temperature. Thermal shutdown protection function could further protect the devices from excessive temperature rise.

10 Application and Implementation

10.1 Application Overview

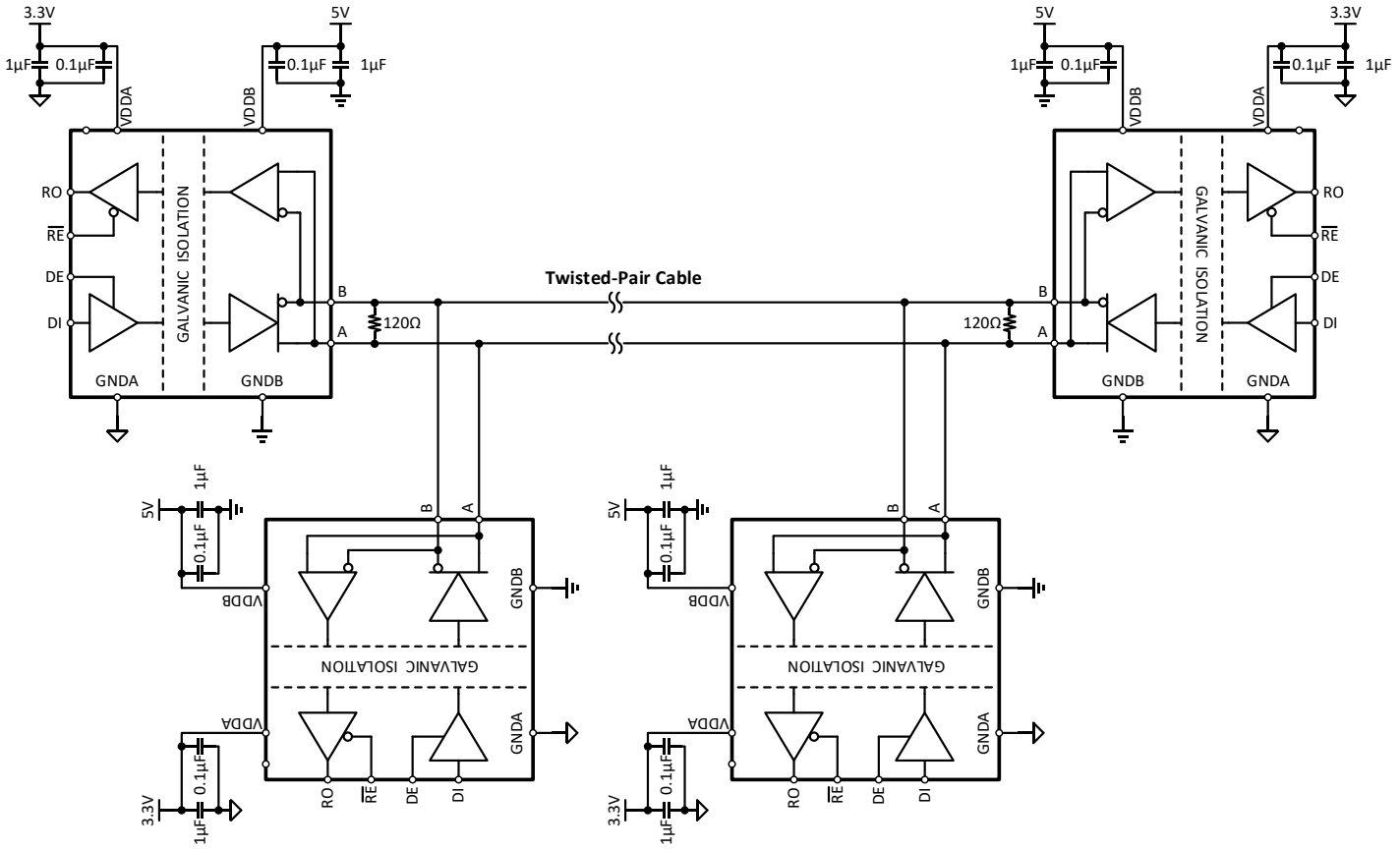


Figure 10-1 Typical Half-Duplex RS-485 Network Topology

The CA-IS3082WW devices are isolated half-duplex RS-485 transceivers. Users could control the driver and receiver enable pins to configure different operation modes and thus avoid bus conflicts. The typical RS-485 network consists of multiple transceivers connecting in parallel to a twisted-pair bus cable, achieving long-distance data transmission between different nodes, which is shown in Figure 10-1.

The maximum data rate of the CA-IS3082WW devices is 500kbps. The maximum data rate achieved in practical applications is limited by the bus loading, number of nodes, cable length, network topology etc. factors. Margin must be given in RS-485 network design for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity. To minimize reflections, terminate the line at both ends with a termination resistor (typical value is 120Ω) whose value matches the characteristic impedance (Z_O) of the cable, and keep stub lengths off the main line as short as possible. The termination resistors should always be placed at the far ends of the cable which is known as parallel termination, generally allowing for higher data rates over longer cable length.

10.2 Bus Node Number

The maximum number of transceivers (or receivers) that the RS-485 bus allows to be attached to depends on the overall load of the system, and any device connected to the bus would introduce additional bus load. RS-485 bus load is usually measured in "unit load" according to the RS-485 standard. With a twisted-pair cable which characteristic impedance is 120Ω (or greater), the bus could be connected to 32 receivers which the input impedance is "unit load" as well as 12kΩ (thus the total bus load is 12kΩ / 32 = 375Ω). The receiver input impedance of the CA-IS3082WW device is 1/8-unit load that is 96kΩ, thus the number of transceivers allowed to be attached to a common bus could reach up to 32 x 8 = 256.

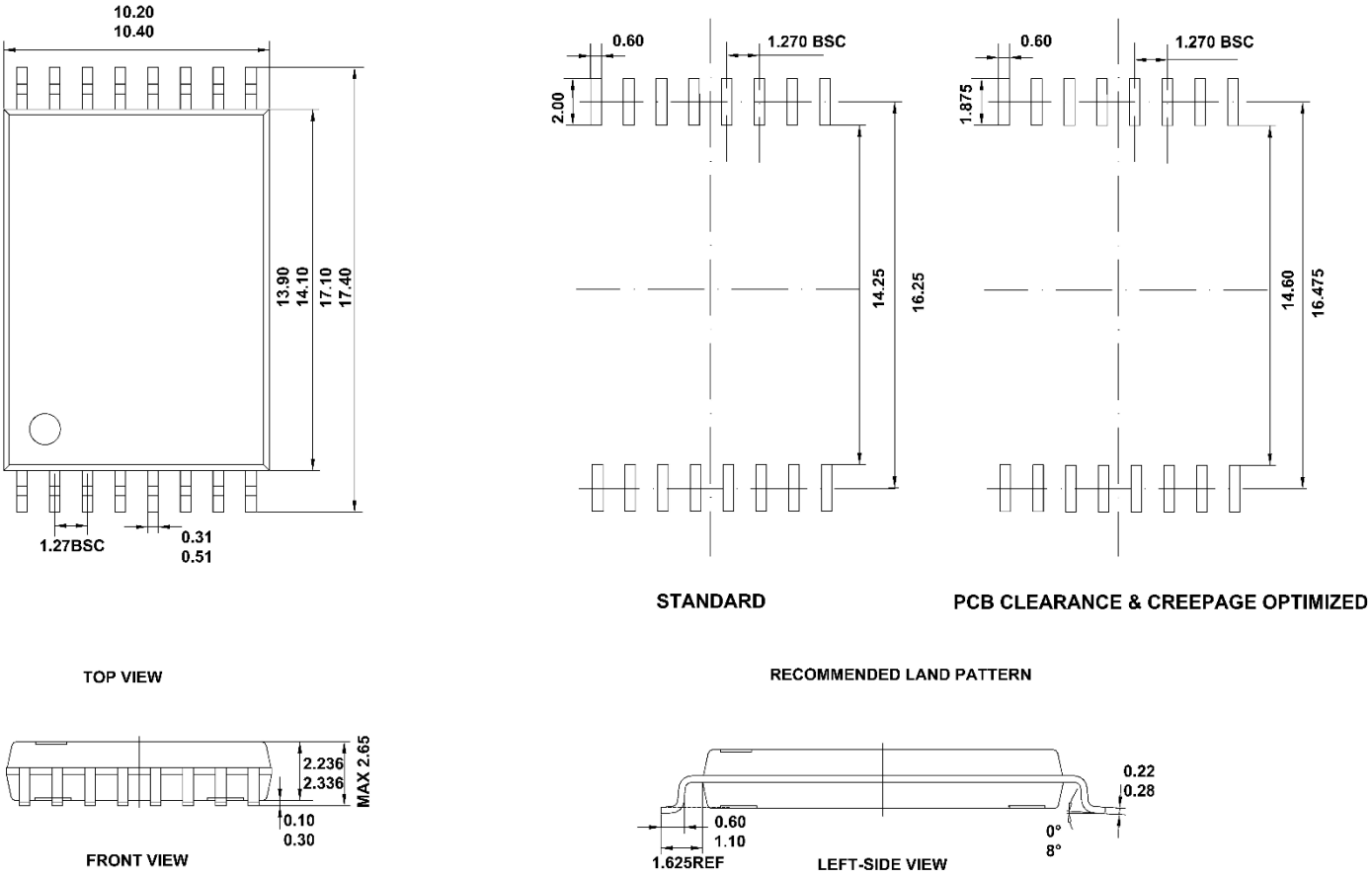
10.3 PCB Layout

It is recommended to design an isolation channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the bus side and logic side would lower down the isolation rating. To make sure device operation is reliable at all data rates, the 0.1-µF and 1-µF decoupling capacitors between VDDA and GNDA and between VDDB and GNDB are recommended. The capacitors should be located as close as possible to the device to minimize inductance and keep the value enough at the operating temperature range. Ceramic capacitors are recommended.

11 Package Information

11.1 SOIC16-WWB Package

The values for the dimensions are shown in millimeters.



12 Soldering Information

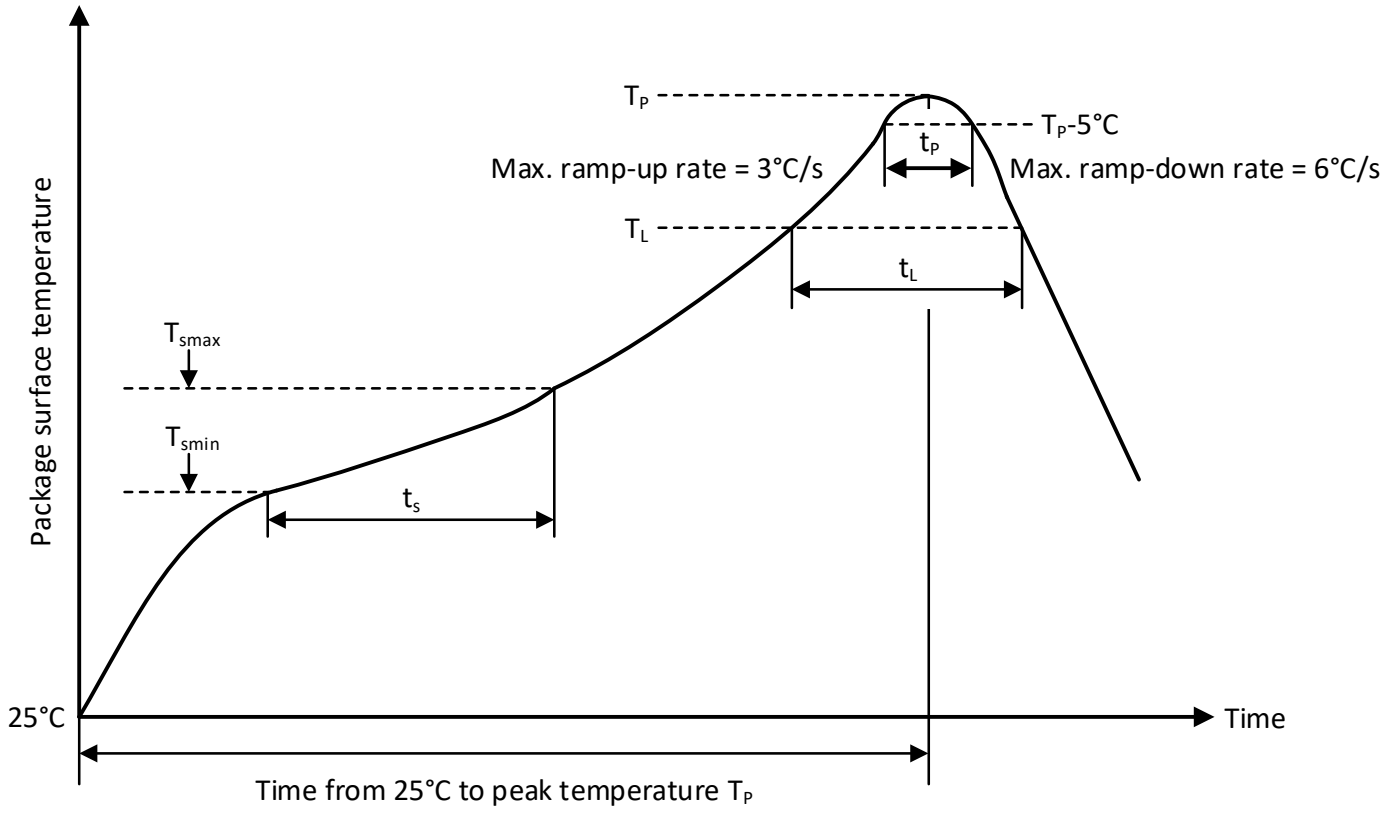


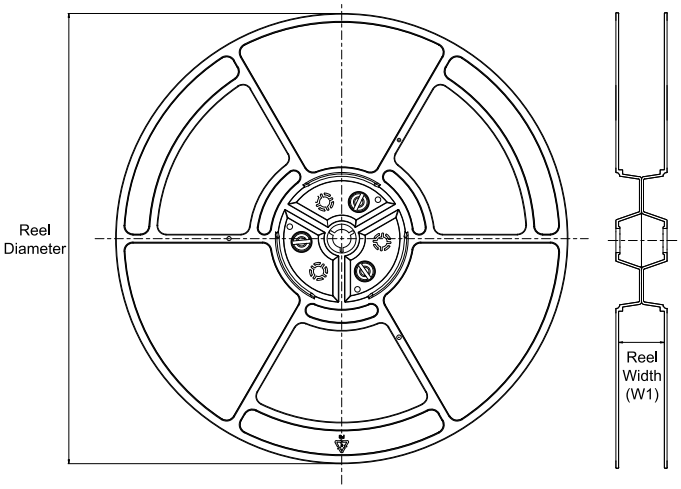
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

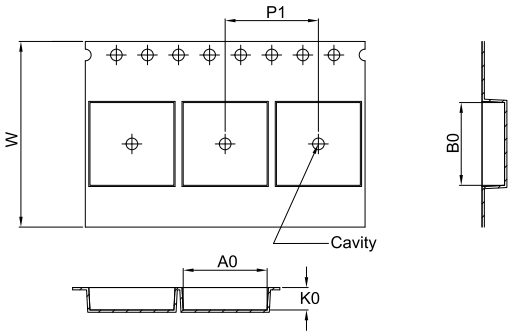
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

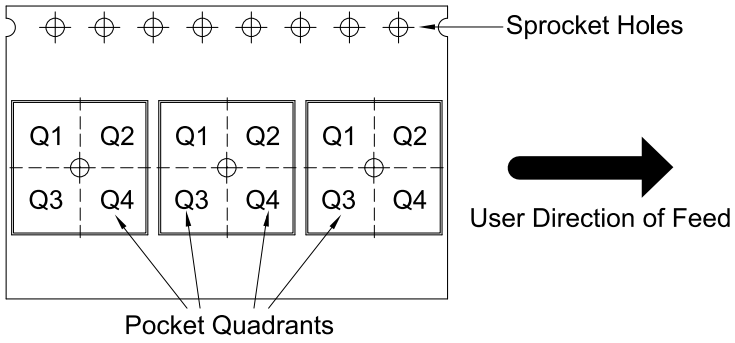


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3082WW	SOIC	WW	16	1000	330	24.4	17.6	10.8	3.0	20.0	24.0	Q1

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